IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Canceled)

Claim 2 (Canceled)

Claim 3 (Canceled)

Claim 4 (Canceled)

Claim 5 (Canceled)

Claim 6 (Canceled)

Claim 7 (Original): A semiconductor device manufacturing method comprising, when one of an N-type and P-type is defined as a first conductivity type and the other is defined as a second conductivity type, the steps of:

forming a first buried layer of the first conductivity type in a vicinity of a surface at inside of one side of a semiconductor substrate of the first conductivity type and forming a second buried layer of the first conductivity type in a vicinity of a surface of the other side, in such a manner that the first and second buried layers sandwich a substrate layer composed of a remaining portion of the semiconductor substrate;

forming first and second base layers of the second conductivity type in a vicinity of surfaces at insides of the first and second buried layers in such a manner that bottom surfaces are positioned in the first and second buried layers; and

forming first and second emitter layers of the first conductivity type in vicinity of surfaces at insides of the first and second base layers so that bottom surfaces thereof are positioned in the first and second base layers.

Claim 8 (Original): The semiconductor device manufacturing method of claim 7, wherein the first and second buried layers are formed by introducing an impurity of the first conductivity type into the semiconductor substrate with surfaces of both sides of the semiconductor substrate completely exposed and diffusing impurity of the first conductivity type.

Claim 9 (Original): The semiconductor device manufacturing method of claim 8, wherein the first and second base layers are formed by introducing an impurity of the second conductivity type into the first and second buried layers with the surfaces of the first and second buried layers completely exposed and diffusing impurity of the second conductivity type.

Claim 10 (Original): The semiconductor device manufacturing method of claim 7, further comprising, with ring-shaped moats having bottom surfaces reaching positions deeper than bottom surfaces of the base layers, a step of forming moats including the first and second emitter layers inside of the ring-shaped moats on both sides of the semiconductor substrate.

Claim 11 (Original): The semiconductor device manufacturing method of claim 10, further comprising a step of forming first and second metal films short-circuiting the first and

second emitter layers positioned inside of the ring-shaped moats and the first and second base layers after filling insides of the first and second moats with oxide and forming first and second passivation films.

Claim 12 (Canceled)

Claim 13 (Canceled)

Claim 14 (Canceled)

Claim 15 (Canceled)

Claims 16 - 20 have been added as follows:

Claim 16 (New): A semiconductor device comprising, when one of either an N-type or P-type is defined as a first conductivity type and the other is defined as a second conductivity type,

a semiconductor substrate of the first conductivity type,

first and second buried layers of the first conductivity type provided within one side and the other side of the semiconductor substrate respectively, and being of a higher concentration than the semiconductor substrate;

first and second base layers of the second conductivity type provided within a surface of the semiconductor substrate nearer to the surface of the substrate than the first and second buried layers, wherein the first and second buried layers form PN junction to the first and second buried layers, respectively;

first and second emitter layers of the first conductivity type, wherein the first and second emitter layers are located in a vicinity of a surface of inside of the first and second base layers so as to form PN junctions with the first and second base layers, respectively,

first and second ohmic layers of second conductivity type and being of a higher concentration than the first and second base layers, wherein the first and second ohmic layers are located in a vicinity of a surface of inside of the first and second base layers,

ring-shaped first moat positioned at the edge portion of regions constituted by the first emitter layer and first ohmic layer, wherein the first moat have a bottom surface deeper than the first base layer and the bottom surface reach the first buried layer,

and ring-shaped second moat positioned at the edge portion of regions constituted by the second emitter layer and second ohmic layer, wherein the second moat has a bottom surface deeper than the second base layer and the bottom surface reach the first buried layer,

wherein the first and second base layers are exposed at a side surface of first and second moats so as to form PN planar junction between the first and second base layers and first and second emitter layers.

Claim 17 (New): The semiconductor device according to claim 16,

wherein first electrode film is provided on the surface of the first emitter layer and the surface of the first base layer so as to short-circuit between the first emitter layer and the first base layer, and second electrode film is provided on the surface of the second emitter layer and the surface of second base film so as to short-circuit between the second emitter layer and the

second base film.

Claim 18 (New): The semiconductor device according to claim 16, wherein the insides of the first and second moats are filled with oxide.

Claim 19 (New): The semiconductor device according to claim 16, wherein at least a part of the first and second base layers are exposed at a surface of a region located outer periphery of the first and second moats.

Claim 20 (New): The semiconductor device according to claim 16, wherein at least a part of the first and second buried layers are exposed at a surface of a region located outer periphery of the first and second moats.